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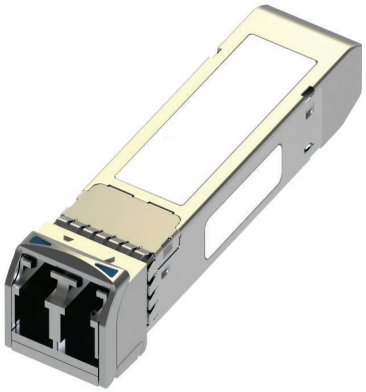
12Gbps Video SFP Optical Dual Receiver, 20km Reach
GRR-12G-L2CD

Features



- ✓ SD/HD/3G/6G/12G-SDI SFP Dual Receiver
- ✓ ST 259, ST 292-1,ST 424, ST-2081 and ST-2082 compatible
- ✓ Metal enclosure for Lower EMI
- ✓ Supports SDI pathological patterns for SD-SDI HD-SDI, 3G-SDI,6G-SDI and 12G SDI
- ✓ With Reclockers in the module
- ✓ ROHS compliant(lead free)
- ✓ single 3.3V power supply
- ✓ Hot-pluggable SFP footprint
- ✓ Operating case temperature range：0 to +70℃

Applications

- ✓ Serial Digital Fiber Transmission System for SMPTE ST 259, SMPTE ST 344, SMPTE ST 292-1/2, SMPTE ST 424, SMPTE ST 2081-1 and SMPTE ST 2082-1 Signals
- ✓ UHDTV/HDTV/SDTV Service Interfaces

Description

CLR Networks Video Receiver is designed to receive data rates from 50Mbps to 11.88Gbps， compliant with SMPTE ST 2082-1 (12G UHD-SDI), ST 2081-1 (6G UHD-SDI), ST424 (3G SDI), ST 292-1 (HD-SDI), and ST 259 (SD-SDI). CLR Networks Video Receiver supports SDI pathological patterns signals.

The Receiver includes these sections: PIN photodiodes integrated with a trans-impedance preamplifier (TIA) , Reclockers , and a MCU controller.

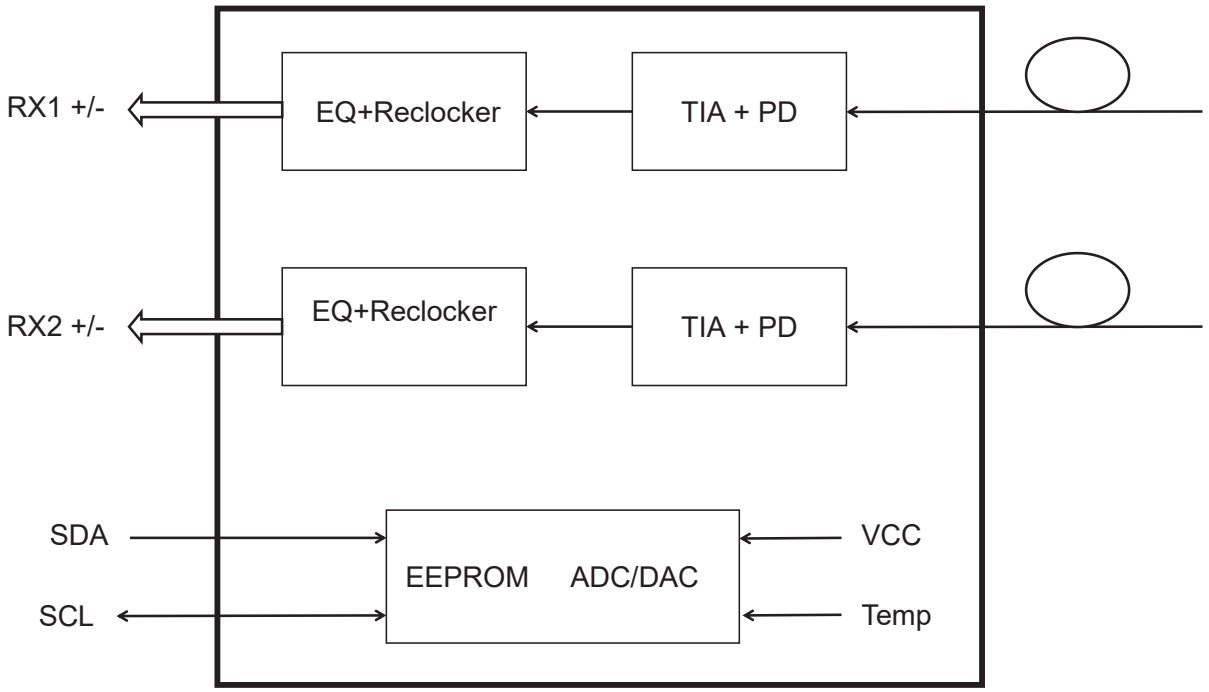


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.5	5．25	V
Storage Temperature	T_s	-40	+85	ºC
Operating Humidity	-	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_c	0		+70	ºC
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc		260		mA
Data Rate			12		Gbps

Optical and Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λ_c	1260		1580	nm	
Receiver Sensitivity@ 11.88Gbps				-11	dBm	1
Receiver Sensitivity@ 5.94Gbps				-13	dBm	
Receiver Sensitivity@ 2.97Gbps				-15	dBm	
Receiver Overload		1			dBm	2
LOS De-Assert	LOS_D			-18	dBm	
LOS Assert	LOS_A	-28			dBm	
LOS Hysteresis	LOS_H	1		4	dB	
Data Output Swing Differential	Vout	400	800	800	mV	3
LOS	High	2.0		Vcc	V	
	Low			0.8	V	

Note:

1. MeasuredWith Pathological Patterns 11.88Gpbs (4096*2160 P60,100% Bars);5.94Gpbs (4096*2160 P29.97,100% Bars);2.97Gpbs (2048*1080 P50,100% Bars).
2. Internally AC-coupled, minimum input overload power for SMPTE ST 2081-1, SMPTE ST 2082-1.
3. Rise and fall times, 20% to 80%

Timing and Electrical

Parameter	Symbol	Min	Typical	Max	Unit
Time To Initialize	t_init			300	ms
Serial ID Clock Rate	f_serial_clock		100		KHz
MOD_DEF (0:2)-High	V_H	2		Vcc	V
MOD_DEF (0:2)-Low	V_L			0.8	V

Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
temperature	0 to +70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
RX Power	-24to +1	dBm	±3dB	Internal / External

I2C Bus Interface

The I2C bus interface uses the 2-wire serial CMOS E2PROM protocol. The serial interface meets the following specifications:

1.Support a maximum clock rate of 280Khz.

2. Input/Output levels comply with LVCMOS/LVTTL or compatible logics.

Low: 0 – 0.8 V

High: 2.0 – 3.3 V

Undefined: 0.8 – 2.0 V

Pin Description

Pin	Signal Name	Description	Plug Seq.	Notes
1	VEE	Receiver ground	1	
2	RX2-	Receiver Inverted Data Output2	3	Note 3
3	RX2+	Receiver Non-Inverted Data Output2	3	Note 3
4	VEE	Receiver ground	3	
5	SCL	SCL Serial Clock Signal	3	Note 1
6	SDA	SDA Serial Data Signal	3	Note 1
7	VEE	Receiver ground	3	
8	NC	Not Connected	3	
9	NC	Not Connected	3	
10	NC	Not Connected	1	
11	VEE	Receiver ground	1	
12	RX1-	Receiver Inverted Data Output1	3	Note 3
13	RX1+	Receiver Non-Inverted Data Output1	3	Note 3
14	VEE	Receiver ground	1	
15	VCC	Receiver Power Supply	2	
16	VCC	Receiver Power Supply	2	
17	VEE	Receiver ground	1	
18	NC	Not Connected	3	
19	NC	Not Connected	3	
20	NC	Not Connected	1	

Note:

Plug Seq: Pin engagement sequence during hot plugging.

1. SDA/SCL . These are the module definition pins. They should be pulled up with a 4.7k~10kΩ resistor on the host to a voltage between 3.13V and 3.46V

SDA is the clock line of two wire serial interface for serial ID.

SCL is the data line of two wire serial interface for serial ID.

2. LOS is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host to a voltage between 3.13V and 3.46V. Logic 1 indicates loss of signal; Logic 0 indicates normal operation. In the low state, the output will be pulled to less than 0.8V.

3. RXn-/+: They are the differential outputs. They are internally AC-coupled 100 differential lines which should be terminated with 100Ω (differential) on the host.

Pin Definition

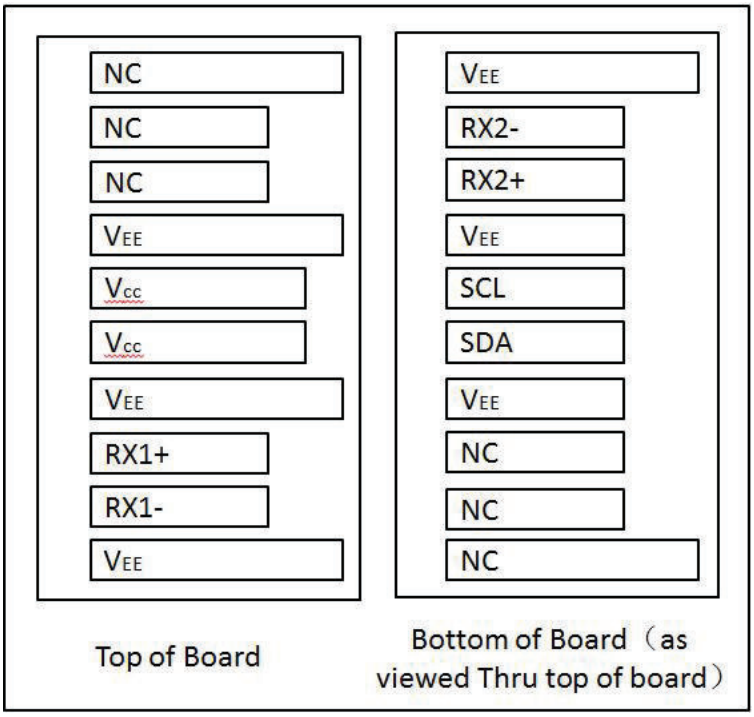


Figure 2. Electrical Pin-out Details

Mechanical Dimensions

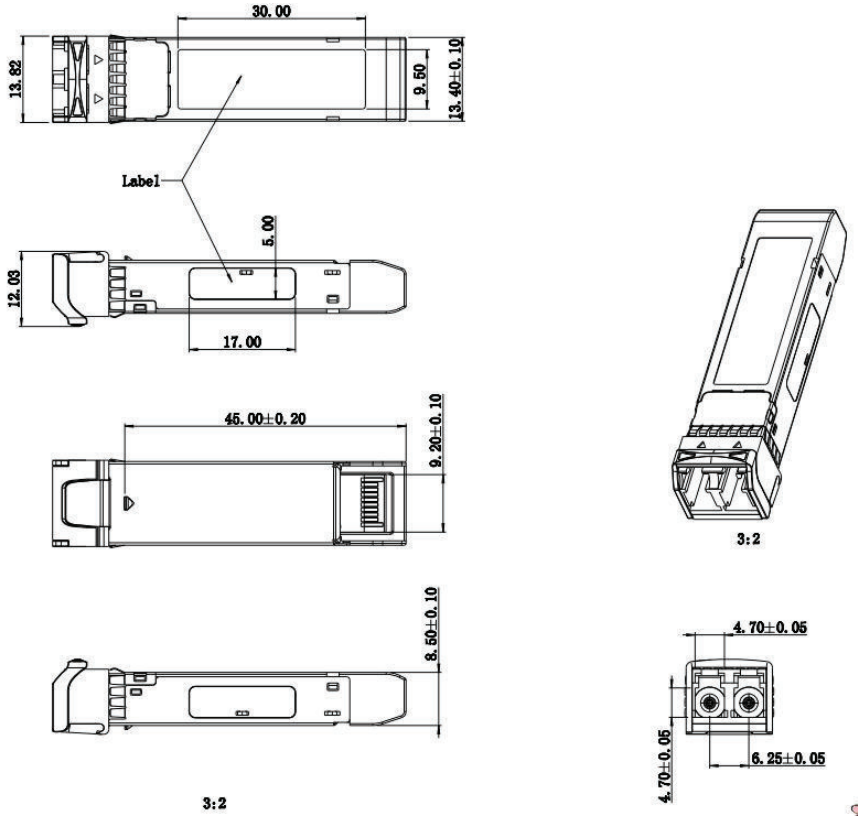


Figure 3. Mechanical Specifications